Final Projects

EE330 – Integrated Electronics

Iowa State University

Spring 2024

Contents

1. Project Policies

1.1 Project Option

This document provides a list of final project options for EE330 students. All final projects require use of Cadence. These projects focus on either digital, analog, or mixed-signal design. Each project is expected to be completed by a two-person team, although if any student prefers to work alone, individual projects are acceptable. If help is needed in finding a partner, please note when signing up for a project.

1.2 Project Assignment

A sign-up link will be provided. This link will ask for the name of both partners if a partner has been identified. Only one of the two partners should sign-up in the link. The sign-up link will allow each group to specify their first, second, and third choices. Attempts will be made to align project assignments with group preferences though this alignment cannot be guaranteed. Individual team members need not be from the same laboratory section. We will restrict the project selection so that at most two teams are working on any one of the projects. If there are more requests for specific projects, assignments will be handled on a first-come, first-serve basis. To help ensure a group gets the project they want, students are encouraged to sign up as soon as possible after the signup link is opened. Once the project is assigned, the team will be will be asked to provide an outline of the project within 1 week. It should include a description of the approach, the block diagram of the circuit that will be designed, and design specs. The team will be expected to discuss the outline with the TA that will be coordinating the project by the end to the first week.

Students who do not choose a project will be assigned to a project and students who do not choose a partner will be assigned a partner if requested. Please read each project description carefully before making a project selection.

1.3 Getting Help

Each project will have a TA associated with it. If there are any questions regarding a project, please contact the TA that is associated with the project.

1.4 Project Expectations

Each project will have four project expectations. These are

Demonstrated Project Checkpoints
Complete Design (schematic and layout)
Project Presentation
Project Report

Project Checkpoints

There will be specific checkpoints for each project. The specific requirements for these checkpoints should be discussed with the TA in charge of the project at the beginning of the project. Checkpoints are assigned to help ensure progress is being made and will have assigned due dates. C**heckpoints should be submitted on Canvas by their due date.** Checkpoints will make up 10% of the final project grade.

Complete Design

All designs should be done in the ON 0.18μm CMOS process. The complete design should include a layout of the circuit including insertion of the project into a pad frame. Though

all students worked on the design of a pad frame in a laboratory experiment, for uniformity, the TAs will provide the pads that can be used to form your pad frame. Post layout simulation results should be used to confirm that the design is complete. Included in your discussions with the TA what post layout simulations you will provide. A major portion of your project grade will be assigned to the successful completion of the design.

Project Presentation

A project presentation should be made to the TAs after the design is complete. Schedule 30 minutes for the project presentation. The first 15 minutes will be a presentation of the design using power point slides. The remaining time will be used to answer questions about your project. These presentations should be scheduled during dead week. The TAs will provide a list of times for the project presentations.

Final Project Report

Students will be asked to submit a final project report which goes through project design. At a minimum, the report should discuss what the design does, how it works, and prove that the design functions with respect to project specifications and constraints. Plots, image, and math should be included as necessary. Treat this project report as one which would be submitted to a boss's boss; it is assumed they have a basic knowledge of what is being done but do not understand any of the specific design details. The goal of the presentation is to inform the boss's boss what the project consists of and that it is functional and practical (to a degree).

The final project report is due at 11:59PM CDT on Friday, May 3, 2024.

2. General Information

2.1 Operational Amplifier

Some projects require, or are greatly helped by, the use of operational amplifiers. Internally compensated op-amp design is beyond the scope in this course but is discussed in EE435 and EE501. So instead, projects which need op-amps will be using externally compensated op-amps. (Do not confuse external op amps with externally-compensated op amps.) A document providing guidance on designing an externally-compensated op-amp has been posted on the class WEB site.

2.2 Comparator

Some projects require, or are greatly helped by, the use of comparators. The design of comparators is not discussed in this course. A document providing guidance on designing a comparator has been posted on the class WEB site.

2.3 Verilog

Digital and mixed-signal projects will require a degree of Hardware Description Language (HDL) knowledge to complete. While TAs will help when necessary, it is expected that students are proactive in learning to use a HDL (likely Verilog will be the HDL of choice) in order to complete a project, where necessary.

3. Projects

3.1 Digital Potentiometer / Programmable Amplifier

This project is for the design of a digital potentiometer / amplifier / DAC integrated circuit. The digital potentiometer is similar in principle to the Maxim DS1666, but with a reduced number of taps, with parallel rather than serial control of the tap position, and with a linear taper rather than an audio taper. The design should include layout and post-layout simulations results. The details of the device to be created are as follows:

The IC will provide the user with 4 functionalities. These are: a programmable non-inverting amplifier, a programmable inverting amplifier, a programmable digital potentiometer, and a DAC. For this project an op-amp will be needed. The operating voltages for the design should be V_{DD} = 2.5V and V_{SS} = -2.5V. There should be one output pin, which will output one of the four functionalities mentioned based on a two-bit mode control signal A_0A_1. Once an option is selected, the output should change appropriately. In addition to the two-bit mode control signal, a four-bit program control input $C_0C_1C_2C_3$ should be provided to control the programmable options. Both the mode control and program control signals should use 2.5V as logic high and -2.5V as logic low. The user inputs should be expected to be both DC and AC signals, so bidirectionality should be integrated in the design. The four functions defined by the two-but mode control signal are described below:

A_0A_1 = 00

The circuit is to perform as a programmable, non-inverting, finite-gain amplifier. The user can provide an input signal along with the four-bit program control input. The output should be an amplified version of the input. The digital potentiometer (discussed below) should be used to control the gain of the amplifier in 16 steps.

A_0A_1 = 01

The circuit is to perform as a programmable, inverting, finite gain amplifier. It is functionally the same as option A_0A_1 = 00, except the output should be inverted.

A_0A_1 = 10

The circuit is to perform as a digital potentiometer. The digital potentiometer should have 16 taps with a nominal impedance between any two adjacent taps of 500Ω. The user should be able to provide a voltage on the upper potentiometer terminal, denoted as $V_{TO\,P,}$ anywhere between -2.5V and +2.5V, and a voltage on the bottom terminal, denoted as V_{BOT}, anywhere between -2.5V and V_{TOP}.

A_0A_1 = 11

The circuit is to perform as a 4-bit buffered output string DAC. The op-amp should be configured as a unity gain buffer in this application. The reference voltage for this DAC, denoted as V_{REF}, should be 1V relative to ground. (The basic digital potentiometer can be configured to form the resistor string for this DAC).

3.2 Torch Light

The term “Torch Light” refers to a flash light that offers a high-intensity output, generally provided by a high-intensity LED. Some of the most practical Torch Lights are powered by a single rechargeable lithium-ion battery.

For this project design an IC that can be used to built a torch light. The torch light should be powered by a single 18650 Lithium Ion Battery and the light source should be a CREE XM-L2 LED. The Torch Light should have 4 user-selected modes of operation.

Mode 1: Constant output at maximum current rating of the LED

Mode 2: Flashing continuously with 50% duty cycle with approximately 2 second spacing between the flash outputs.

Mode 3: Constant output at low intensity (defined to be average power to be approximately 10% of that in Mode 1)

Mode 4: Morris Code Mode. Outputs pulse sequence of SOS in Morris Code.

There should be 2 switches. One is a Power On switch (SPST) and one is a mode select (SPSTM).

At Power On, it should enter Mode 1. Every time the mode select switch is pushed the Mode should be advanced by 1.

3.3 Temperature Sensor with Digital Output

This project is for the design of an integrated, low power, linear temperature sensor with a two decimal-digit output over a temperature range of 0°C to 99°C. The design should include layout and post-layout simulation results.

Digital temperature sensors are used in many devices. They work using the output of temperature dependent devices such as diodes. The design can make use of resistors and diodes/silicon (or substrate BJTs) to generate the basic VBE voltages and Proportional to Absolute Temperature (PTAT) voltage and will likely require an op-amp. Design the circuit to use V_{DD} = 2.5V and V_{SS} = -2.5V

The temperature should be displayed on a two-digit 7-segment display (alternately you can use two digits of a three-digit or a four-digit display). The exact type of display that will be used for the design (i.e. a commercial part number) should be specified. The circuit should be designed to drive the display directly without the need for any additional, external components. It is likely that a simple Analog to Digital Converter (ADC) will be needed to convert between the analog PTAT voltage and two-digit 7-segment display output.

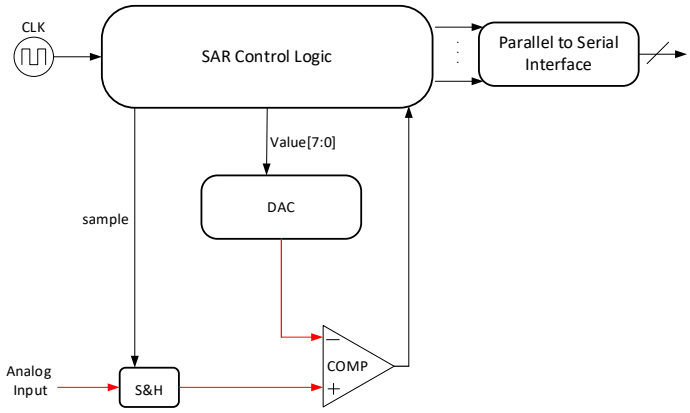
3.4 Class D Audio Amplifier

This project is for the design of a class-D audio amplifier that can drive an 8Ω speaker. The circuit should have 6 pins, VDD, Gnd, Vin+, Vin- ,Vout+, Vout-. The speaker should be connected directly across the output port pins. The switches in the class-D amplifier should be sized so that the power dissipation for a 500mW speaker output is less than 10mW.

3.5 Serial Output SAR Analog-to-Digital Converter

This project is for the design of an analog-to-digital converter which has an 8-bit serial output. Analog-to-digital converters serve as vital components which can convert an analog signal to a digital signal. Analog signals can include reflected light, vibrations, RF transmissions, air pressure, etc. Some everyday items which utilize ADCs include computer mice, televisions, and microphones.

A successive approximation ADC (SAR) works by using a digital-to-analog converter (DAC) and a comparator to perform a binary search to find the input voltage. A sample and hold (S&H) is used to sample the analog input voltage and hold (i.e. keep a non-changing copy) the sampled value whilst the binary search is being performed. The binary search starts with the most significant bit (MSB) and works towards the least significant bit (LSB). For example, an 8-bit output resolution requires 8 comparisons in the binary search, taking at least 8 clock cycles. An op-amp may be needed in your design. The ADC should have a reference voltage of V_{REF}=1V relative to ground and the input to the ADC should satisfy the relationship $0<V_{IN}<V_{REF}$.



For this design, it is assumed that logic high is 2.5V and logic low is -2.5V. The transmission of an ADC reading should be triggered by an external signal. When the ADC is not transmitting data, the output should be held in a constant state. The data may be transmitted in 12-bit packets, where the first two and last two bits represent start/stop bits, and the middle eight bits are the data to be transmitted. The clock should be external to the design, and the serial transmission should be in sync with the provided clock.

One important block of the SAR ADC is a comparator. Basically, the comparator output is logic 1 if the sampled analog voltage is greater than the output of the DAC and zero otherwise. The controller should have control and status signals and indicate when conversion is complete, and the result which is an 8-bit serial output data should be shown.

The use of a HDL to design the SAR logic controller may be beneficial. The result should include a synthesized schematic with simulation results that prove device operation. A layout should be included, along with valid DRC and LVS results.

3.6 Digital Alarm with Battery Backup

This project is for the design of a digital alarm with battery backup. The time should be displayed on a four digit seven-segment display.

You should specify a specific commercial display (i.e. part number) that will comprise the display output. During normal operation, the time base should be derived from the 60 Hz line voltage. Assume an external transformer is available to generate a 60Hz signal from a standard 120V supply line at whatever amplitude you specify. The battery back up should keep the clock functioning when power is lost. Although the frequency of the 60Hz line voltage is very precisely controlled so if the clock is "Set" correctly, the time can be very precise, when operating in battery backup mode, the time-base accuracy need only be accurate to +/- 30%. If power is lost and then comes back again, the 60 Hz line voltage should again serve as the time reference. Since the accuracy of the time will be degraded when operating in the battery backup mode, it will be assumed that the user will need to reset the clock after a battery backup event occurs. A separate LED light should be lit whenever battery backup mode is first entered and should remain lit until the clock is reset. Two output pins should be provided to drive a buzzer when the alarm goes off. Specify the specific commercial buzzer that the circuit is intended to drive. You may add up to four switches for the purpose of setting the clock or operating the alarm.

3.7 4B/5B Encoder for Serial Data Communications

When data is being transmitted serially between two systems, it is invariably impractical to transmit a clock signal yet the receiving system must know when to sample the incoming signal and how to identify the starting point of each packet of data. A clock recovery circuit is used in the receiver to synchronize the incoming serial data stream. Most clock recovery methods depend on measuring time between data level transitions and utilizing a phase-locked loop to accurately capture sent data. However, if there are not a sufficient number of transitions in the transmitted data (e.g. data = 0000 or data = 1111), clock recovery becomes difficult, if not impossible, and data will be lost.

An 8B/10B data encoding scheme is often used to encode 8B data for serial data transmission. With an 8B/10B encoding scheme, each 8B byte is mapped to a 10B word that is rich in data transitions for any 8B input. Though it represents a 25% overhead in the number of bits transmitted, it does provide a sufficient number of data transitions to allow recovery of the clock signal that was used at the transmitter. A fixed number of the 10B data words are then concatenated into packets of data along with a header sequence and a stop sequence to comprise a frame. The frame header allows for synchronization of the 10B words in the

receiver. For this project, a 4B/5B encoding scheme is used instead of an 8B/10B scheme strictly to reduce the size of the logic needed for the encoder.

A 4B/5B encoding scheme can also be designed to reduce or eliminate data loss by ensuring there are at least two transitions in every four-bit data frame. To accomplish this, four-bit data is mapped to a five-bit code, and data is transmitted in packets with five-bit data frames. This allows the phase-locked loop to stay in sync for the duration of data transmission.

For this design, the supply voltages are V_{DD} = 2.5V and V_{SS} = -2.5V. Logic high should be 2.5V and logic low should be -2.5V. It should be assumed that the encoder has both a serial input and serial output. The encoder output should be a differential pair. A packet should be 20 bits, consisting of two five-bit start codes, one five-bit data frame, and one five-bit stop code. An external clock may be provided to the encoder.

The use of a HDL to design the logic may be beneficial. The result should include a synthesized schematic with simulation results that prove device operation. A layout should be included, along with valid DRC and LVS results.

3.8 Simple Calculator

This project is for the design of a simple calculator which can perform a mathematical operation on any three-digit number. The calculator must be able to add, subtract, multiply, or divide, depending on the state of the operation control bits, the three-digit number by any integer between 0 and 9, inclusive. If the resulting number is fractional, it should be rounded down. The results of the performed mathematical operation should be provided as output to a 12-pin four digit seven-segment display and stored to memory. You should specify a specific commercial display that will comprise the display output.

In the case that a divide-by-zero error is encountered, the seven-segment display should show dashed lines. Mathematical operations should be selected using a two-bit control input. An additional control bit should be included to implement reset functionality. Further, a “LOAD” bit should exist which can be used to load the previous result from memory into the three-digit input. If the number stored in memory is greater than four digits, the first digit should be dropped to ensure the loaded number is only three digits.

This project will necessitate using HDL to describe the system. The result should include a synthesized schematic with simulation results that prove device operation. A layout should be included, along with valid DRC and LVS results. Additional credit may be awarded for added functionality with prior TA approval.

3.9 Voice Controlled Light Controller

This project involved the design of an integrated circuit in a 0.5u CMOS process that can be used to control a Triac for turning on lights in response to several types of inputs as described below. The design should be complete through post layout simulation.

The controller should handle up to a 500 watt load with power supplied by the standard 120V 60Hz line voltage. Assume you have available a 5V dc power supply, two commercial photo-transistors or a photo-resistors, and a commercially available microphone. You must specify exactly which photodetector, microphone, and Triac you will use.

If the ambient light level is above a predetermined value, the lights should be able to be turned on with a SPST switch but if the ambient light level is below this predetermined value, the SPST should not be able to turn the lights on. Pressing the SPST when the lights are on should always turn the lights off. If the light level is below the predetermined level, they should be turned on by a voice command. When activated by voice command, they should turn off automatically after 30 seconds after the last recognized voice command unless turned off by the SPST. If the light level is below the predetermined level, they should be also turned on by a laser input to a photo-detector. When turned on by a laser input, they should turn off automatically after 10 sec after the last laser input unless turned off by the SPST